R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

Applicants thank Examiner Lee for the indication of allowable matter for claims 5-8 and 13-16.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments and new claims may be found in the specification, for example, on page 11 lines 8-14, FIG. 4 and claims 5 and 13, as originally filed. Thus, no new matter has been added.

CLAIM OBJECTIONS

The objection to claims 5-8 and 13-16 for dependency upon rejected base claims has been obviated by appropriate amendment and should be withdrawn. Each of claims 5 and 13 have been rewritten into independent form and include portions of the original claims 5 and 13 believed to be the reason for allowance as cited on page 5 of the Office Action. The remaining portions of the original claims 5 and 13 have been moved to new claims 18-21. As such, claims 5-8 and 13-16 are now in a condition for allowance and the objection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4, 9-12 and 17 under 35 U.S.C. §102(b) as being anticipated by Miller '822 has been obviated in part by appropriate amendment, is respectfully traversed in part and should be withdrawn.

Miller concerns a semaphore circuit for shared memory cells (Title). In contrast, claim 1 provides (in part) a controller configured to set a semaphore to a busy status in response to a processor reading a first address while the semaphore has a free status. Miller appears to be silent regarding setting a semaphore status in response to a **read**. In particular, Miller appears to contemplate switching the status of a semaphore circuit 10 in response to processors **writing** to registers 20 and/or 22. Therefore, Miller does not appear to disclose or suggest a controller configured to set a semaphore to a busy status in response to a processor reading a first address while the semaphore has a free status as presently claimed.

Claim 1 further provides a free status, a grant status and a busy status. In contrast, Miller appears to be silent regarding a free status, a grant status and a busy status. associated with the semaphore circuit 10. Therefore, Miller does not appear to disclose or suggest a free status, a grant status and a busy status as presently claimed. Claim 9 provides language

similar to claim 1. As such, claims 1 and 9 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 17 provides means for setting a semaphore to a busy status in response to presenting a granted status. Despite the assertion on page 2 of the Office Action, the semaphore circuit 10 of Miller appears to be silent regarding the claim limitation. In particular, the semaphore circuit 10 of Miller appears to be silent regarding a structure which sets the semaphore circuit 10 to a "busy" status in response to a latch 24, a latch 26, a mux circuit 14 and/or a mux circuit 16 presenting a "granted" status. To the contrary, Miller appears to contemplate **presenting** semaphore information **in response to setting** the status of the cross-coupled NOR gates 50 and 52 within the semaphore circuit 10. Therefore, Miller does not appear to disclose or suggest a means for setting a semaphore to a busy status in response to presenting a granted status as presently claimed. The Examiner is respectfully requested to either (i) explain how Miller discloses **setting** a busy status **in response to presenting** a granted status or (ii) withdraw the rejection.

Claim 17 further provides a free status, a grant status and a busy status. In contrast, Miller appears to be silent regarding a free status, a grant status and a busy status. associated with the semaphore circuit 10. Therefore, Miller does not appear to disclose or suggest a free status, a grant status and

a busy status as presently claimed. As such, claim 17 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 3 provides a controller configured to present a status of a semaphore in response to (from claim 1) a processor reading a first address and (from claim 3) the processor reading a second address. In contrast, a mux circuit 16 of Miller appears to disclose only one unique address on lines 118, 122 and 124 for accessing each of the semaphore circuits 10-12. For example, only one input to MUX 150, and thus only one address, appears to route data from a latch 26 within the semaphore circuit 10 to a data I/O line 142 in Miller. Therefore, Miller does not appear to disclose or suggest a controller configured to present a status of a semaphore in response to a processor reading a first address and the processor reading a second address as presently claimed. Claim 11 provides language similar to claim 3. As such, claims 3 and 11 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 depends from claim 3 and provides that the controller is further configured to maintain the status of the semaphore in response to the processor writing to the second address. As noted above for claim 3, Miller appears to be silent regarding each semaphore circuit 10-12 being accessible through two addresses. Therefore, Miller does not appear to disclose or

suggest a controller configured to maintain a status of a semaphore in response to a processor writing to a second address as presently claimed. Claim 12 provides language similar to claim 4. As such, claims 4 and 12 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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Dated: July 29, 2004

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Docket No.: 01-669 / 1496.00169